

Exhibit IV

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Engineering & Materials: Electrical & Electronics

Engineering: Physical electronics

Transistor

A solid state device involved in amplifying small electrical signals and in processing of digital information. Transistors act as the key element in amplification, detection, and switching of electrical voltages and currents. They are the active electronic component in all electronic systems which convert battery power to signal power. Almost every type of transistor is produced in some form of semiconductor, often single-crystal materials, with silicon being the most prevalent. There are several different types of transistors, classified by how the internal mobile charges (electrons and holes) function. The main categories are bipolar junction transistors (BJTs) and field-effect transistors (FETs).

Single-crystal semiconductors, such as silicon from column 14 of the periodic table of chemical elements, can be produced with two different conduction species, majority and minority carriers. When made with, for example, 1 part per million of phosphorus (from column 15), the silicon is called *n*-type because it adds conduction electrons (negative charge) to form the majority carrier. When doped with boron (from column 13), it is called *p*-type because it has added positive mobile carriers called holes. For *n*-type doping, electrons are the majority carrier while holes become the minority carrier. For *p*-type doping holes are in larger numbers, hence are the majority carriers, while electrons are the minority carriers. All transistors are made up of regions of *n*-type and *p*-type semiconducting material. See also: Semiconductor; Single crystal

The bipolar transistor has two conducting species, electrons and holes. Field-effect transistors can be called unipolar because their main conduction is by one carrier type, the majority carrier. Therefore, field-effect transistors are either *n*-channel (majority electrons) or *p*-channel (majority holes). For the bipolar transistor, there are two forms, n^+pn and p^+np , depending on which carrier is majority and which is the minority in a given region. As a result the bipolar transistor conducts by majority as well as by minority carriers. The n^+pn version is by far the most used as it has several distinct performance advantages, as does the *n*-channel for the field-effect transistors. (The n^+ indicates that the region is more heavily doped than the other two regions.)

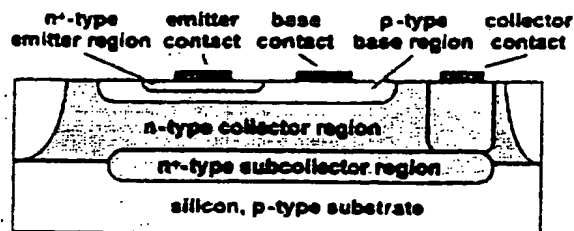
Bipolar transistors

Bipolar transistors have additional categories: the homojunction for one type of semiconductor (all silicon), and heterojunction for more than one (particularly silicon and silicon-germanium, $\text{Si}/\text{Si}_{1-x}\text{Ge}_x/\text{Si}$). At present the silicon homojunction, usually called the BJT, is by far the most common. However, the highest performance (frequency and speed) is a result of the heterojunction bipolar transistor (HBT).

Bipolar transistors are manufactured in several different forms, each appropriate for a particular application. They are used at high frequencies, for switching circuits, in high-power applications, and under extreme environmental stress. The bipolar junction transistor may appear in discrete form as an individually encapsulated component, in monolithic form (made in and from a

common material) in integrated circuits, or as a so-called chip in a thick-film or thin-film hybrid integrated circuit. In the pn -junction isolated integrated-circuit n^+pn bipolar transistor, an n^+ subcollector, or buried layer, serves as a low-resistance contact which is made on the top surface (Fig. 1). See also: Integrated circuits; Junction transistor

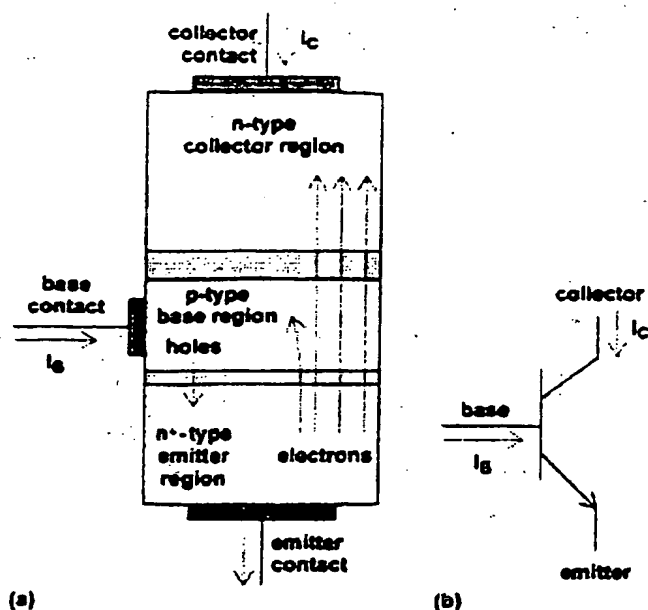
Fig. 1 Isolated n^+pn bipolar junction transistor for integrated-circuit operation.



Basic operation

The n^+pn bipolar transistor (Fig. 2 a) has three differently doped regions and two junctions, the emitter-base junction and the collector-base junction, in a single crystal of silicon. It is possible to describe a large part of bipolar transistor operation by interpreting the device somewhat like a pair of back-to-back diodes. The emitter-base junction is usually forward-biased; that is, the voltage of the base with respect to the emitter, V_{BE} , is greater than 0. This voltage is small (less than 1 V), but the forward current across the junction is relatively large, just as in the forward-biased diode. The majority carriers in the emitter region (n^+ -type) are electrons. These are injected across the emitter-base junction into the base region (p -type), which is quite thin, being on the order of 0.1-0.5 micrometer. With the base-collector junction reversed-biased (that is, the voltage of the collector with respect to the base, V_{CB} , is greater than 0), the holes that are present in the p -type base material do not cross it, as they are repelled by the electric field from the collector. However, the electrons that have been injected from the emitter into the very thin base region (where they become minority carriers) diffuse across the base-collector junction and are then collected under the influence of the positive collector potential (Fig. 2 a). This electron current across the base-collector junction is almost as large as the electron current crossing from the emitter into the base region. In general, it runs from 99.5 to 99.99% of the emitter current, the small decrease being accounted for by electrons that are lost in the narrow base region. In terms of electron currents, for every 200 electrons flowing into the emitter from the external contact and crossing into the base region, perhaps one causes a current in the base lead, whereas 199 cross over into the collector and flow out into the external collector circuit. See also: Diffusion; Junction diode; Semiconductor diode

Fig. 2 Operation of an n^+pn bipolar junction transistor. (a) Conceptual cross section with carrier flows. (b) Circuit symbol.



The total current across any junction results from both hole and electron motion. In the emitter, electrons are injected from the n^+ region into the p region of the base, while holes are injected from the p -type base back into the emitter. These holes also cause current to flow into the base lead. The sum of these two currents crossing the junction determines the total emitter current. Even though holes and electrons flow in opposite directions, they add together as total current. However, in the emitter-base junction this hole current is usually several orders of magnitude less than the electron current, a consequence of much heavier doping in the emitter region compared to the base. The total base current is made up of two small components: the holes injected from the base to the emitter, and the electrons lost from the emitter due to recombination in the base. It is desirable for the base current to be as close to zero as possible, in order to obtain large current gains from base to collector.

Circuit symbol

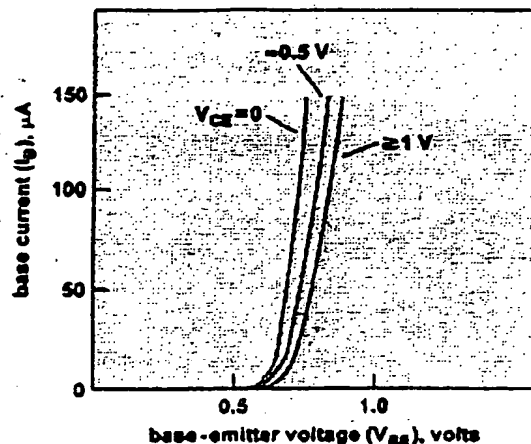
The circuit symbol for an n^+pn bipolar transistor (Fig. 2b) has an arrowhead on the emitter lead whose direction indicates that electrons flowing in from the emitter to the base are the same as if positive charges were leaving that terminal. Hence, the arrowhead points out of the emitter.

Voltage-current characteristics

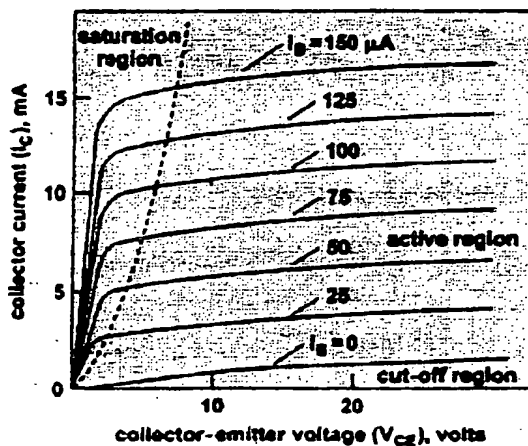
The input voltage-current characteristics of an n^+pn transistor (Fig. 3 a) are a family of curves of base current, I_B , versus base-emitter voltage, V_{BE} , for various values of collector-emitter voltage, V_{CE} . The output characteristics (Fig. 3 b) are curves of collector current, I_C , versus collector-emitter voltage, V_{CE} , with the base current, I_B , as an independent parameter. These curves display two general characteristics. First, once the collector-emitter voltage is greater than 1 or 2 V, the collector current is relatively independent of this voltage; that is, each curve flattens out. Second, in this region the collector current is about 100 times the base current. The ratio of collector current to base current with the collector base voltage, V_{BE} , equal to zero is defined as the dc beta (β_{dc}) for the bipolar transistor.

Fig. 3 Voltage-current characteristics of a typical low-power n^+pn bipolar transistor. (a) Input

characteristics: base current (I_B) versus base-emitter voltage (V_{BE}) for various values of collector-emitter voltage (V_{CE}). When $V_{CE} > 1$ V, the curves coincide. (b) Output characteristics: collector current (I_C) versus collector-emitter voltage (V_{CE}) for various values of base current (I_B). (After W. H. Hayt, Jr., and G. W. Neudeck, *Electronic Circuit Analysis and Design*, 2d ed., reprint, Wiley, 1995)



(a)



(b)

The voltage-current characteristics emphasize the regions where the emitter-base junction is forward-biased (the base-emitter voltage, V_{BE} , is greater than 0) and the collector-base junction is reverse-biased (the collector-base voltage, V_{CB} , is greater than 0). These bias conditions define the active region for a bipolar transistor, which is mainly used for analog circuits. A quick glance at the input characteristics shows that the base current is greater than 0 under these conditions. When both junctions are reverse-biased, any currents that flow are several orders of magnitude smaller, and this is termed the cutoff region ("off" for digital circuits). The condition that both junctions are forward-biased defines the saturation region or the "on" region for digital circuits. Both the base-emitter voltage, V_{BE} , and the base-collector voltage, V_{BC} , are small positive values; and the collector-emitter voltage, V_{CE} , their difference, is also small and positive. The boundary between the active and saturation regions occurs where the collector-base voltage, V_{CB} , equals 0.

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The p^+np transistor contains a narrow n -type base layer sandwiched between p -type emitter and collector regions. Forward bias on the emitter-base junction causes holes to be injected into the base region, most of which diffuse across the thin base and are collected by the reverse-biased base-collector junction. The total emitter current, I_E , is thus composed of the sum of this large hole current plus a much smaller electron current directed from the base toward the emitter.

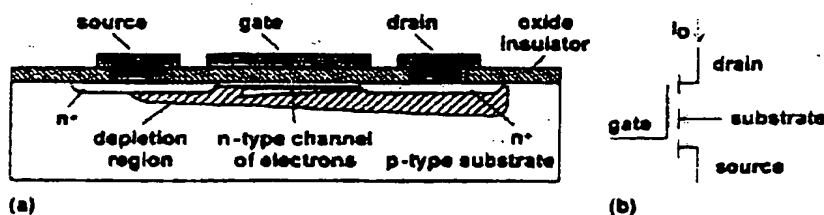
Field-effect transistors

Majority-carrier field-effect transistors are classified as metal-oxide-semiconductor field-effect transistor (MOSFET), junction "gate" field-effect transistor (JFET), and metal "gate" on semiconductor field-effect transistor (MESFET) devices. MOSFETs are the most used in almost all computers and system applications. However, the MESFET has high-frequency applications in gallium arsenide (GaAs), and the silicon JFET has low-electrical noise performance for audio components and instruments. In general, the n -channel field-effect transistors are preferred because of larger electron mobilities, which translate into higher speed and frequency of operation.

MOSFETs

An n -channel MOSFET (Fig. 4) has a so-called source, which supplies electrons to the channel. These electrons travel through the channel and are removed by a drain electrode into the external circuit. A gate electrode is used to produce the channel or to remove the channel; hence it acts like a gate for the electrons, either providing a channel for them to flow from the source to the drain or blocking their flow (no channel). With a large enough voltage on the gate, the channel is formed, while at a low gate voltage it is not formed and blocks the electron flow to the drain. This type of MOSFET is called enhancement mode because the gate must have sufficiently large voltages to create a channel through which the electrons can flow. Another way of saying the same idea is that the device is normally "off" in a nonconducting state until the gate enhances the channel.

Fig. 4 An n -channel enhancement-mode metal-oxide-semiconductor field-effect transistor (MOSFET). (a) Cross section. (b) Standard circuit symbol.



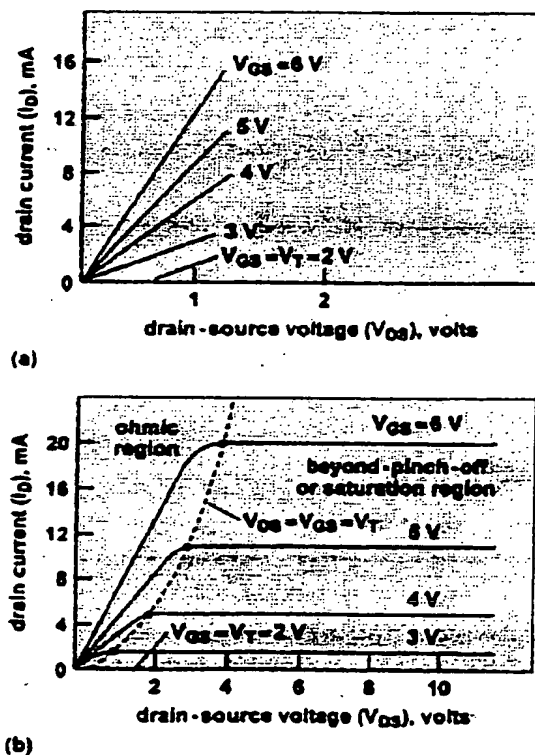
An n -channel MOSFET with a positive gate-source voltage, V_{GS} , and a small drain-source voltage, V_{DS} , has an electric field established across an insulating layer (Fig. 4). This field acts to repel positive carriers (holes) in the substrate and to attract negative carriers (electrons). As a result, a layer of substrate near the insulator becomes less p -type and its conductivity is reduced. As the gate-source voltage increases further, this surface region of the substrate eventually has more electrons than holes, and it inverts to n -type. Additional increases in gate voltage add more electrons to the channel and make it even more conductive. This n -channel (Fig. 4a) now conducts electrons from the n^+ source to the n^+ drain which has a positive voltage and attracts electrons. Between the p -type substrate and the n -type channel is a depletion (transition) region that serves to isolate the substrate from the channel, a process referred to as self-isolation. Since conduction is by electrons, the majority carrier, the MOSFET is a majority-carrier device.

The smallest value of the gate-source voltage, V_{GS} , that will produce a channel and a resultant value of drain current, I_D , greater than the few nanoamperes is called the threshold voltage, V_T , typically 0.2-2 V. V_T output voltage-current characteristics of the device are a family of curves of drain-current, I_D , versus drain-source voltage, V_{DS} , for several values of gate-source voltage, V_{GS} (Fig. 5). When the drain-source voltage is small (Fig. 5 a), the device behaves as a voltage-controlled linear resistance. When the drain-source voltage becomes sufficiently large (Fig. 5 b), the gate-to-drain voltage is less than the threshold voltage, that is, Eq. (1)

$$V_{GD} = V_{GS} - V_{DS} \leq V_T \quad (1)$$

holds, and pinch-off occurs at the drain end of the channel. Further increases in drain-source voltage do not lead to larger values of drain current, (that is, the current saturates), since the transistor is operating in the region beyond pinch-off. In this region of operation the MOSFET device behaves as a voltage-controlled current source.

Fig. 5 Output characteristics of n -channel enhancement-mode MOSFET: drain current (I_D) versus drain-source voltage (V_{DS}) for various values of gate-source voltage (V_{GS}). (a) Small values of V_{DS} , where the device behaves as a voltage-controlled linear resistance. (b) Complete output characteristics. (After W. H. Hayt, Jr., and G. W. Neudeck, *Electronic Circuit Analysis and Design*, 2d ed., reprint, Wiley, 1995)



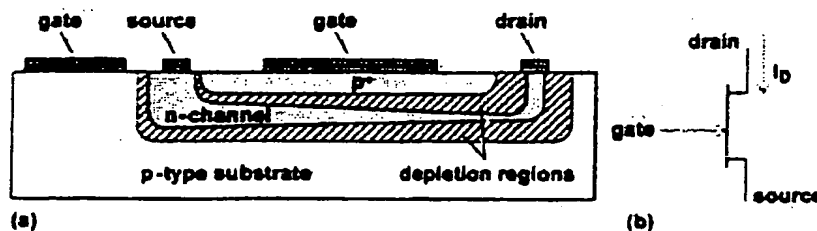
The standard circuit symbol for the n -channel enhancement-mode MOSFET (Fig. 4b) shows the substrate as a separate connector. An arrow shows the direction from the p side (substrate) to the n side (channel) of the junction, while a segmented line indicates the enhancement mode; no channel is present until channel enhancement occurs at which point the gate-source voltage exceeds the threshold voltage.

The p -channel enhancement-mode MOSFET is the complement of the n -channel device. It has an n -type silicon substrate in which a p -type channel is induced (enhanced) by making the gate sufficiently negative that the gate-source voltage is less than the threshold voltage. The gate of a p -channel enhancement-mode MOSFET has an electric field between the gate and substrate which pushes out electrons, attracts holes, and eventually inverts the channel to p type. Now holes conduct between the p^+ source and drain electrodes.

JFETs

In the JFET (Fig. 6 a), a conducting majority-carrier n channel exists between the source and drain. When a negative voltage is applied to the p^+ gate, the depletion regions widen with reverse bias and begin to restrict the flow of electrons between the source and drain. At a large enough negative gate voltage (symbolized V_p), the channel pinches off. The standard circuit symbol (Fig. 6 b) has a continuous bar since current flows with zero gate-source voltage, V_{GS} , at larger values of the drain source voltage, V_{DS} .

Fig. 6 An n -channel junction field-effect transistor (JFET). (a) Cross section. (b) Circuit symbol.



MESFETs

The MESFET is quite similar to the JFET in its mode of operation. A conduction channel is reduced and finally pinched off by a metal Schottky barrier placed directly on the semiconductor. Metal on gallium arsenide is extensively used for high-frequency communications because of the large mobility of electrons, good gain, and low noise characteristics. Its cross section is similar that of the JFET (Fig. 6a), with a metal used as the gate. See also: Schottky barrier diode

High-frequency transistors

High-frequency effects for the bipolar transistor are characterized by the emitter charging time (τ_e), the collector charging time (τ_c), the minority-carrier transit time through the active base region (τ_b), and the base-collector depletion region transit time (τ_{cb}). The emitter charging time equals the product of the emitter-base capacitance (proportional to the area of the emitter) and the thermal voltage divided by the dc current. The minority-carrier transit time through the active base region is approximately the square of the active width of the base region divided by twice the diffusion constant for the minority carriers that diffuse through the base. (The dependence on the active width indicates the need for a very thin base region.) The transit time through the collector-to-base depletion region equals the width of this region divided by twice a saturated velocity to which the carriers can accelerate. Thus, a short transit time requires a large saturated velocity or a small width, which means a small value of the collector-to-base voltage. The final term for the collector is its charging time, approximately the product of the collector contact resistance and the collector-base capacitance. A short charging time thus requires a small value of the former and a small collector area to reduce the latter.

Figures of merit

A figure of merit for the advanced bipolar transistor is the frequency, f_T , at which the short-circuit, current-signal gain is unity. This frequency equals the inverse of the sum of the four times discussed above, τ_e , τ_b , τ_c , and τ_c . A large value of f_T indicates that the intrinsic device is fast.

A more circuit-oriented figure of merit is f_{\max} , the maximum frequency that gain can still be achieved in a circuit, given by Eq. (2).

$$f_{\max} \cong \sqrt{\frac{f_T}{8\pi R_b C_{cb}}} \quad (2)$$

Here the external base resistance, R_b , is important, as well as the base-collector area needed to reduce the collector base capacitance, C_{cb} .

Most very high speed logic circuits belong to the emitter-coupled logic (ECL) family of circuits or the current-mode logic (CML) family. The figure of merit for this type of circuit is given by Eq. (3), where R_c is the collector resistance,

$$\tau_{cs} = 1.7 \sqrt{\frac{(R_c + 2R_b)(3C_{cb} + C_{cs})}{2\pi f_{T\max}}} \quad (3)$$

C_{cs} is the collector-substrate capacitance of the integrated bipolar transistor, and $f_{T\max}$ is the peak value of f_T when the collector current is varied. Again, this expression indicates the need for thin base regions, small emitter and collector areas, and low values of resistances contacting the device. See also: Logic circuits

Structural improvements

The function of the sub-collector in the integrated-circuit bipolar transistor (Fig. 1) is to reduce the collector resistance. Typical values of the current gain, that is, the dc beta, range from 80 to 300, and f_T ranges from 5 to 45 GHz with values of f_{\max} up to 450 GHz. In an emitter-coupled logic circuit the transistor has a gate delay of as low as 15 picoseconds. An improvement to this structure is to reduce the sidewall components of capacitance with the local-oxidation-of-silicon (LOCOS) structure. In addition, a polysilicon-contacted emitter can be added to improve the dc beta, and the external base resistance can be reduced by increased base doping, somewhat similar to what is done in heterojunction bipolar transistors.

Single, self-aligned transistor

The single self-aligned bipolar transistor (SST) reduces the emitter area to $0.35 \times 5 \mu\text{m}$ and has f_T values up to 20 GHz and a dc beta of 180. The use of a pedestal collector and double self-alignment improves the value of f_{\max} and the emitter charging time by reducing the area and the external parasitic resistances. In all these cases the fabrication methods strive to reduce the area, hence the capacitances.

Heterojunction bipolar transistor

The heterojunction bipolar transistor is made from two different types of semiconductor material. The most promising is the silicon-germanium type. It is produced by epitaxially growing a

narrow band-gap base region of heavily doped p -type $\text{Si}_{1-x}\text{Ge}_x$ on an n -type silicon collector and then capping it with an n^+ type silicon emitter. The silicon-germanium compound suppresses the base-injected holes (Fig. 2), and at the same time this allows the base to be doped very heavily to reduce the external base resistance. By grading the germanium content and the doping, f_T values up to 32 GHz and f_{max} of 120 GHz have been achieved, with good values of beta. The circuit delay is about 20 ps. Other heterojunction bipolar transistors of interest include those using the compound semiconductors GaAlAs/GaAs, InGaP/GaAs, and InGaAs/InP. These devices have achieved f_T values of 37 GHz and f_{max} of 90 GHz with powers of 1-5 W. See also: Semiconductor

High-frequency field-effect transistors

The inability of the MOSFET to conduct large currents into capacitive loads has limited its use in extremely high-frequency circuits. However, because of its low power consumption it can be integrated into very dense circuits. The first requirement is that the channel length be small (approximately 1 μm), as it controls how fast the majority carrier can traverse between the source and drain. The carrier mobility must also be large; hence, electrons are preferred, as their mobility is typically two to three times larger than holes. A second requirement is for low values of source and drain resistance. In circuit applications a small value of capacitance between the gate and drain is necessary to reduce the total effective capacitance that is multiplied by the circuit voltage gain. Self-aligned gates, polysilicon, and channel lengths of less than 0.15 μm are used. Typical performance characteristics for a 0.5- μm gate length are an f_T of 10 GHz and an f_{max} of 15 GHz. In complementary metal-oxide-semiconductor (CMOS) circuits with gate lengths of 0.15 μm , gate delays as low as 21 ps per stage are possible.

The more advanced techniques use silicon-on-insulator (SOI) technology to further reduce the external parasitic capacitances around the source and drain. Other device structures include the high electron mobility transistor (HEMT), silicon-germanium MOSFETs, and combinations of bipolar transistors and MOSFETs (BiCMOS). Each technology has its particular advantages. The HEMT is produced from compound semiconductors and can yield an f_T of 300 GHz with gate delays of 25 ps. See also: Microwave solid-state devices

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Models

Whether the transistor is used in the design of small analog circuits or very large scale integrated circuits, its behavior has to be adequately understood by the designer. Analysis of the circuit is a prerequisite to its fabrication, thus pointing to the need for models. The higher levels of integration as well as of the cost of fabrication have increased the need for more accurate models and also their complexity. Circuit simulation programs have become rather commonplace and generally available for use on personal computers. The usefulness of such computer-aided design programs is directly influenced by the accuracy of the transistor models and their adequacy for the design application. In general the models can be categorized as large-signal (nonlinear) models used for dc or transient analysis, and small-signal (linear) models used for ac or frequency-domain analysis.

Most large-signal models are represented by systems of equations relating currents and charges to terminal voltages. Different equations are typically used for different combinations of terminal voltages or regions of operation.

In many analog circuits, the signals are small enough that the nonlinear models can be replaced

by linearized equivalent circuit models. Linear circuits are much less complicated to analyze than nonlinear ones. The hybrid- π configuration can be used for linear modeling of field-effect transistors of bipolar junction transistors. See also: Amplifier; Circuit (electronics); Electrical model

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BIBLIOGRAPHY

- W. H. Hayt, Jr., and G. W. Neudeck, *Electronic Circuit Analysis and Design*, 2d ed., 1984, reprint 1995
- Institute of Electrical and Electronics Engineers, *1994 International Electron Devices Meeting Technical Digest*, San Francisco, California, December 11-14 1994
- G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE*, 2d ed., 1998
- G. W. Neudeck, *The Bipolar Transistor*, 2d ed., 1989
- G. W. Neudeck, *The P-N Junction Diode*, 2d ed., 1989

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